

# Microcomputer Central Processing Unit Module

O. B. Parham

Radio Frequency and Microwave Subsystem Section

*A new multipurpose microcomputer central processing unit (CPU) module is described and illustrated in this article. The module is designed to stand alone and also be upward expandable.*

## I. Introduction

A multipurpose stand-alone microcomputer in one standard DSN logic packaging subchassis (Ref. 1) has been designed for use in the Spectral Signal Indicator (SSI), the Noise Adding Radiometer (NAR), and the Precision Signal Power Measurement (PSPM) projects.

## II. Configuration and Implementation

The three major parts of the microcomputer module are the central processing unit (CPU), the memory, and the input/output (I/O) as shown in the photo (Fig. 1). At the heart of the CPU is an 8080 microprocessor (Ref. 2), which with its support circuitry runs at a 2-MHz clock speed. Additional CPU implementations are a 4-channel direct memory access (DMA) controller for high-speed data transfer between the memory and I/O sections, and an 8-level priority interrupt controller for handling asynchronous events on an interrupt basis. (For a simplified block diagram of the module, see Fig. 2.)

The memory section is comprised of 12 K bytes of erasable programmable read-only memory (EPROM) for program storage and 4 K bytes of random access memory (RAM) for data

storage. To insure the multipurpose nature of the module, the EPROM section of memory incorporates the features necessary to allow the EPROMs to be programmed without being removed from the module. The RAM section of memory is implemented with parity error detection. Thus, should a memory error occur in the RAM area, an interrupt is generated to the CPU, notifying it that the memory has made an error. Additionally, when an error is detected, the upper half of the address bus is latched and can tell the processor which page of memory caused the error.

Components of the module's input/output structure are:

Two RS-232 ports with software controlled transmission rate, or baud rate

Nine parallel 8-bit ports for general-purpose usage

One IEEE-488 interface for interfacing to commercial equipment

One DSN interface for communication with station controllers

In addition to the data I/O, a three-section software controlled counter timer has been implemented. The first two sections of

the timer are cascaded and connected to the interrupt controller to generate real-time interrupts, with the interrupt periods programmable from 2  $\mu$ s to 2147 s. The third section is available for external use as a pulse generator or event counter.

The priority interrupt controller assigns the highest internal priority interrupt (Level 0) to memory parity error detection. The other internal priority interrupts are:

Level 1, to the real-time counter

Level 2, to the DSN interface, the IEEE-488 interface, and the DMA controller

Level 3, to the general-purpose I/O and the RS-232 ports

Four lower priority interrupts (levels 4, 5, 6, 7) are available externally. Internal priority interrupt levels shared between various ports on the same levels are individually maskable by software. The external interrupts are maskable in the interrupt controller.

### III. System Expansion

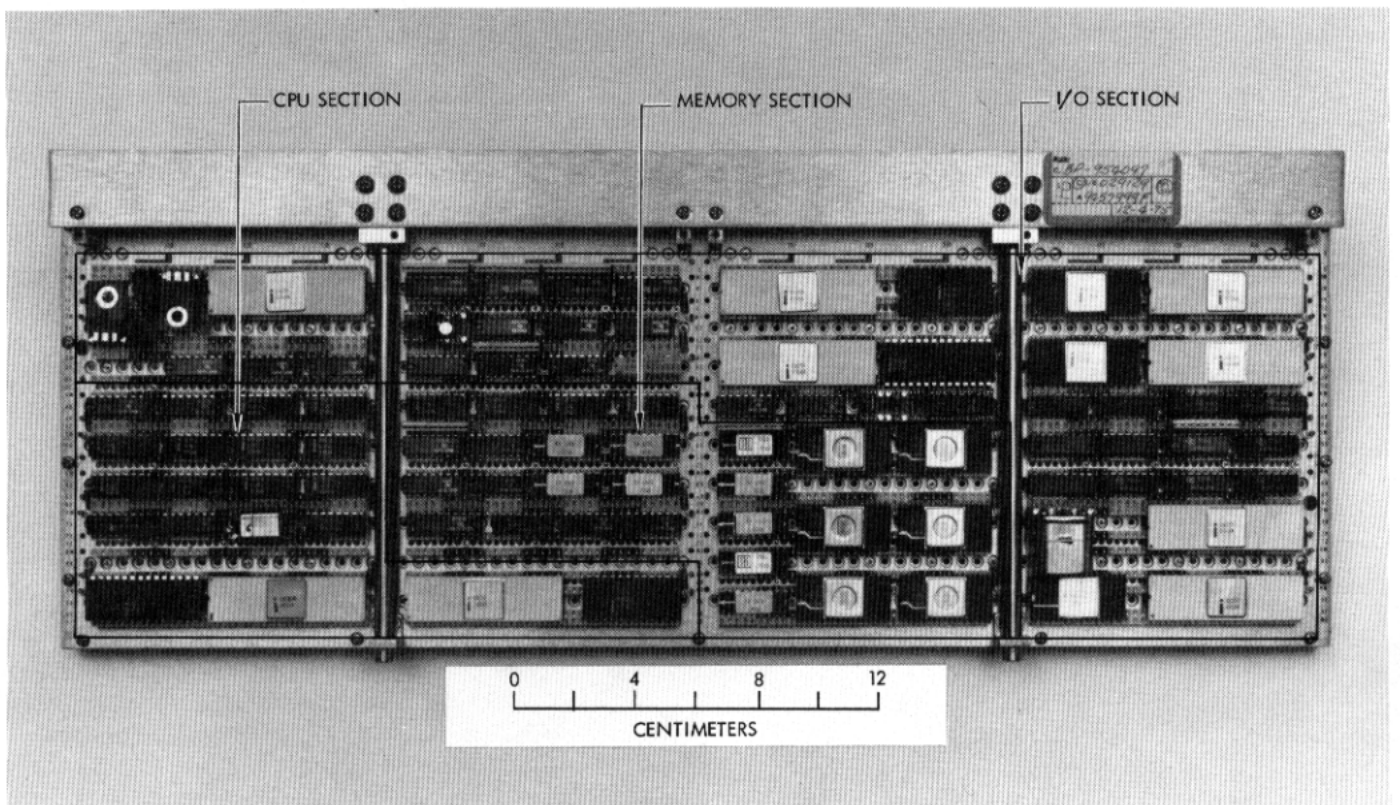
Many applications require more memory and I/O than is available on the microcomputer module. To overcome this, the CPU bus has been buffered and brought out of the module. This allows simple, easy expansion of the system to the full capability of the 8080 CPU. A local memory disable feature has also been incorporated to allow for memory paging. This extends the memory capability beyond the normal 65 K limit of the 8080.

### IV. Summary

A microcomputer module has been designed for use of the NAR, PSPM, and SSI projects. The multipurpose nature of the module will allow it alone, or with expansion modules, to meet the needs of many future DSN requirements.

## References

1. Slaughter, D. W., "Standard High-Reliability Integrated Circuit Logic Packaging," in *The Deep Space Network Progress Report 42-39*, pp. 130-156, Jet Propulsion Laboratory Pasadena, Calif., March and April, 1977.
2. 8080 Microcomputer Systems User's Manual, Intel Corp., Santa Clara, Calif., July 1975.



**Fig. 1. Microcomputer CPU module**

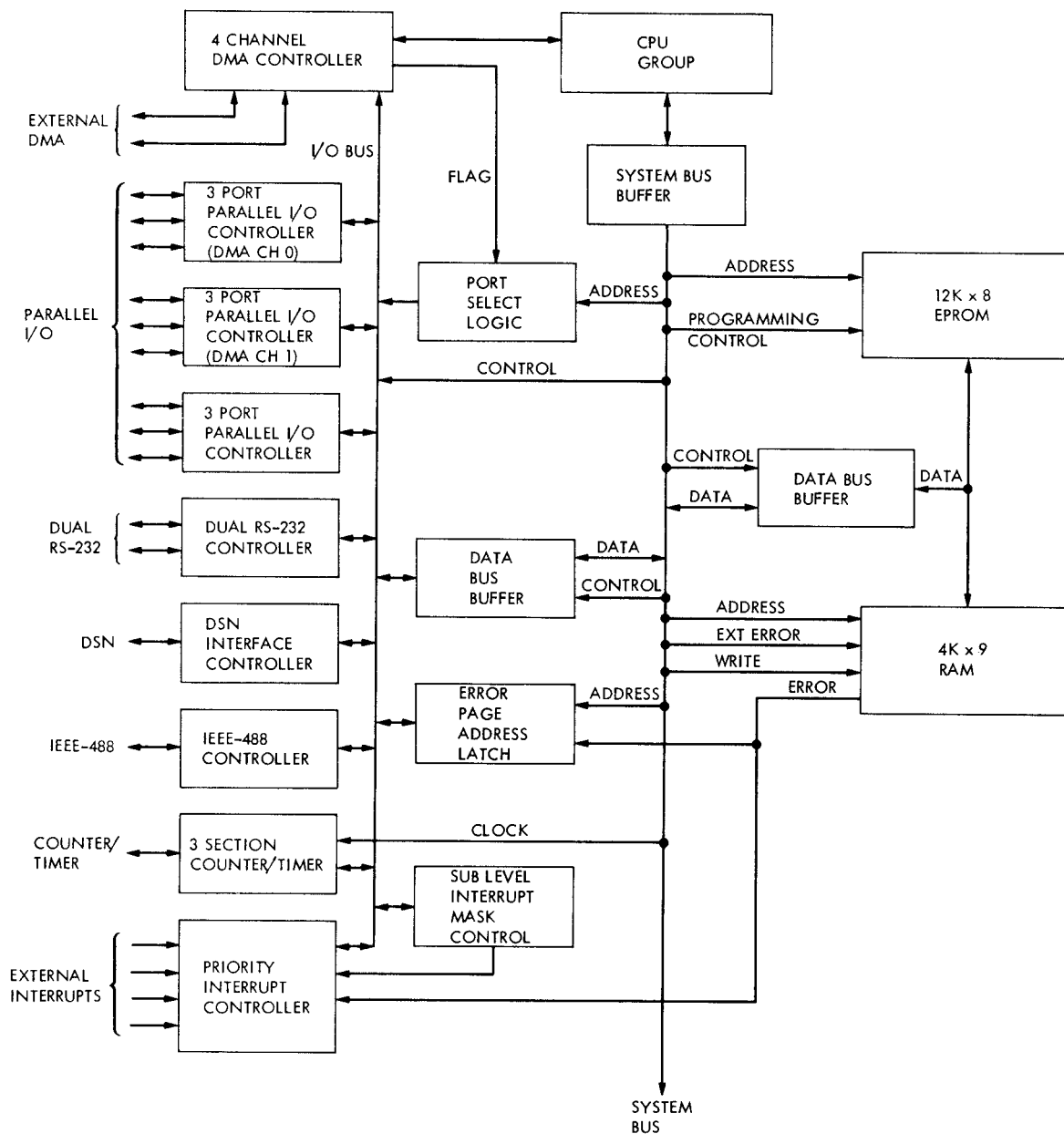


Fig. 2. Simplified block diagram of microcomputer CPU module